* Math Again
- P = VI

3.3V - 14a, 5V - 32a 12V - 8a

46.2 w, 100 w, 96 w = 252.6 w

** Parts

	12V	5V	3.3a	
fans	0.1a			CPU - 25a at 3.3V
H.D.	2.9a	0.9a		
SCSI CR	0.5a	5.0a	7.6a	
CDROM	1.5a	1.0a		
EISA	1.5a	9.5a	7.6a	
PCI	0.5a	5.0a	17.6a	
AGP	19.2a			
MoBo	1.0a	7.0a		(no sound or video)

** Homework

	12V	5V	3.3V
- MB	1.0a	7.0a	
- RAM			2.0a
- HD	2.9a		
- 2 case fans	0.3a		
- sound (PCI)	0.5a	5.0a	7.6a
- video (AGP)	9.2a		7.6
- net (PCI)	0.5a		
- VCC (PCI)	0.5a		
- CPU			25V
- DVD-ROM	3.0a	2.0a	
- floppy	2.9a		7.6a
	20.8a	25.8a	54.8a

$P_{12} = 20.8_a \cdot 12V = 250\ w$

$P_5 = 25.8_a \cdot 5V = 129\ w$

$P_{3.3} \quad 51.8_a \cdot 3.3 = 171$

$P_T = 550\ w$

Safety Rules

** AC + DC
- non-conductive shoes
- no work on power supplies
- jewelry - no-no.
- 300 ma is lethal, voltages as high as 35,000
- don't touch unfamiliar wires or components

** ESD
- electrostatic discharge
- not felt until over 2000V
- computer chips operate at 5V or less
- use wrist straps in computer work

** General Safety
- black wire - hot
- white wire - neutral
- red wire - positive lead in AC, DC is positive lead
- no loose clothing
- sharp edges
- safety glasses (only monitors)
- natural fibers only
- 50% - 60% humidity
- no sudden changes on comp temperature
- no magnetic tools
- surg protectors - prevents changes in current
- power strip -
- uninterrupted power supply - crossover - keeps electricity on, no surg protect
  continuous - comps run off battery

- case, MB, and power supply must match with each other
- tower: full, mid, mini
- different size & capacity
- bays & slots

* desktop
- regular
- low profile - less slots
- almost all proprietary

* motherboard
- AT
- baby AT
- ATX
- micro ATX

> I/O panel

* Power Supplies
- ATX is smaller also known as switching PS
- AC alternates 60 times a second
- must be plugged in
- soft switch
- the button turns the MB off
- voltages are +3.3V, +12, -12, +5, -5 or DC
- CT voltages has all but +3.3V
- +12V for motors, -12V for certain bus, +5V for general purpose circuits, +3.3V for CPU + RAM
- orange wire is AT 3.3V

* PS Service
- 70%, heavy - 60%, mid - 50%, light

- logical is logical and physical tells function
- 4 physical buses
- (depends) logical buses
- speed of original AGP was 66 MHz
- EISA is 16-bits
- AGP x 2 is 33 MHz
- L1 cache is in processor, L2 outside
- AGP is part of front side bus
- 1 bit at a time in serial
- more than 1 bit is parallel
-

* * Physical Buses
- power bus
- control bus
- data bus
- address bus
* * logical Bus
- processor bus
- I/O bus - ISA, PCI, AGP, MCA, EISA, VL
- storage bus -
- USB + IEEE 1394
- memory bus
- I/O - 8.3 MHz
- ISA - 8.3 MHz
- speed is 8.3 MHz, bandwidth depends
- I/O - serial - 8.3 Mb/s - 1 MB/s
- ISA - 64 Mb/s, 8 MB/s
- EISA - 8.3 MHz 16 MB/s
- VL bus - 33 MHz
- PCI - peripheral connector interface, 33 MHz, 4 bytes at a time
- 8086 - first 16-bit processor
- PCI - 133 MB/s
- PCI 2.1 - 33 MHz -
- AGP - accelerated graphics port - 66 MHz - 4 bytes - 266 MB/s
- AGP x 2 - double pump - 533 MB/s, 8 bytes
- PCI 2.2 - 66 MHz 8 bytes, 533 MB/s
- AGP x 4 - quad pumped, 66 MHz, 4 bytes - 1 GB/s

- AGP x 8, 2 GB/s, quad pump 66 MHz, 8 bytes

CPU

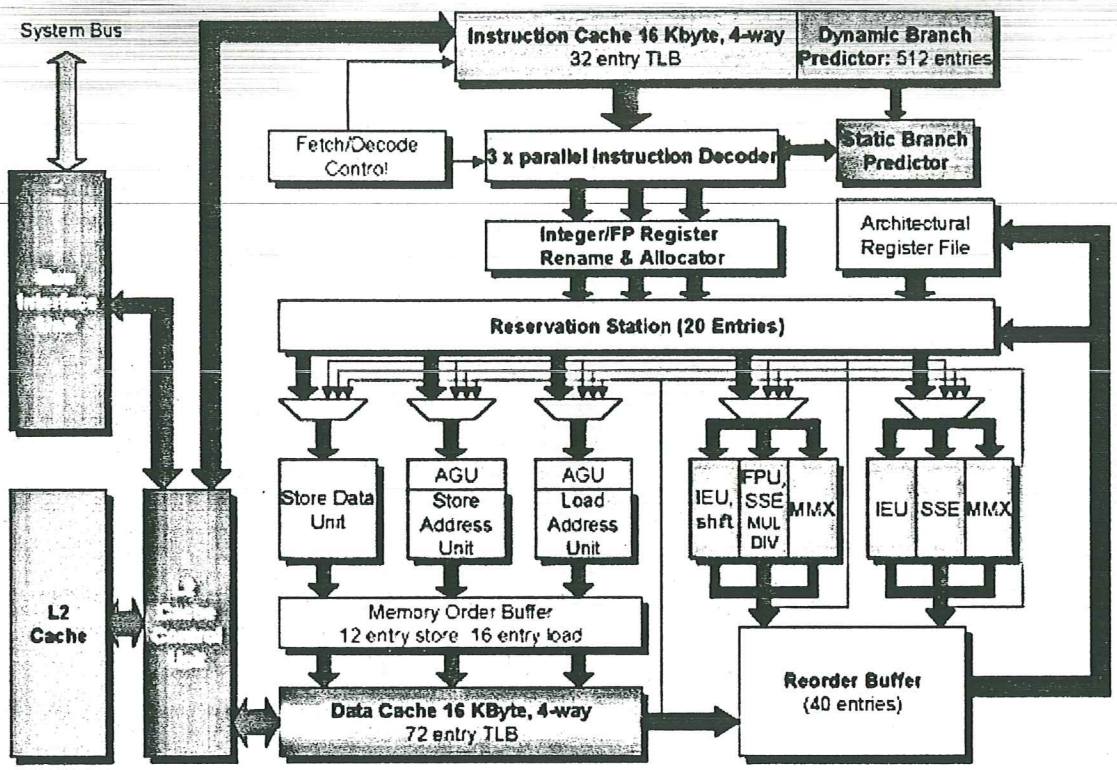
* * CPU

- central processing unit
- 4004 - early processor - 4 bit
- processor - data width - internal registers - address bus
- looking at intel only (x86 is intel)

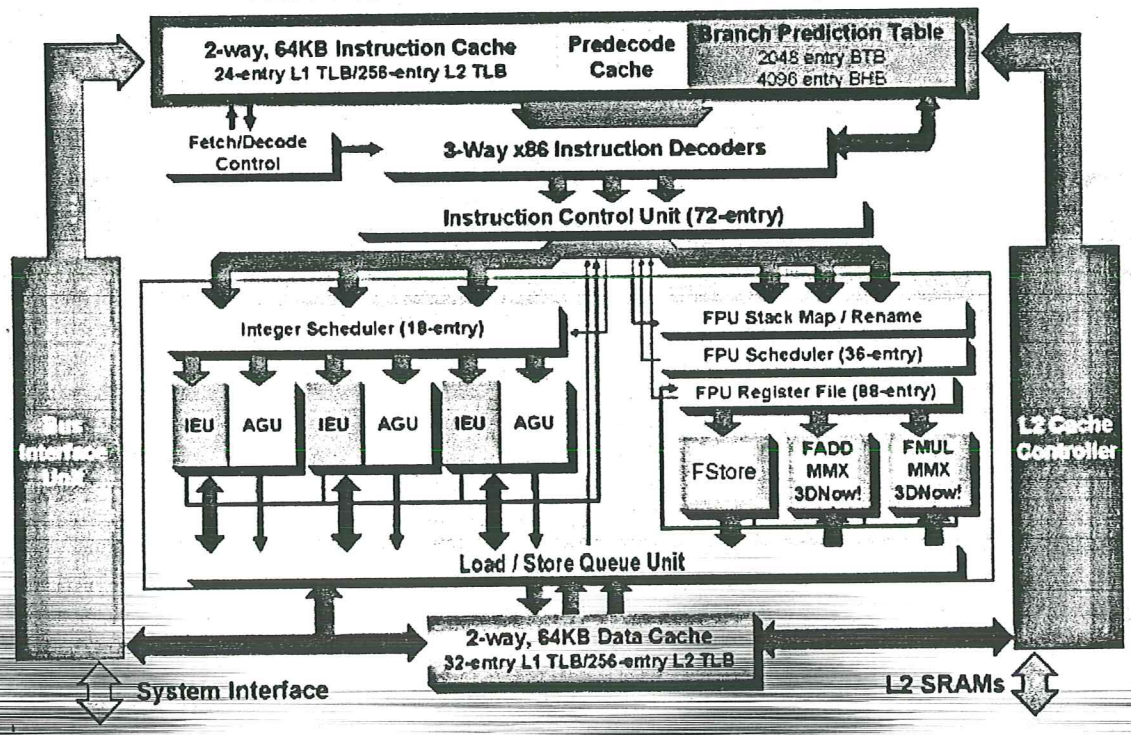
	(intel) processor	data width	address bus	internal registers
1978	8086	16 bits	20 bits	16 bits
1979	8088	8 bits	20 bits	16 bits
	80186	scrapped	because of new technology	
	80286	16 bits	24 bits	16 bits
	80386 DX	32 bits	32 bits	32 bits
	80386 SX	16 bits	32 bits	32 bits → L1 cache 8k
	80486 DX			1x
	80486 DX2	32 bit	32 bit	32 bit 2x
	80486 DX4			3x
P54	80586 (pentium)	64 bit	32 bit	32 bit → split cache 8K data, 8K opt
* P55		" "	" "	" " → MMX 16K-16K split cache
	pentium pro	64 bit	36 bit	32 bit - 8K-8K L1+L2 16K 512K slot A
	pentium II			

- 386 had FPU (floating point unit)
- ALU (arithmetic logic unit)
- 386SX - no internal FPU
- 80387 - chip - external FPU
- 80486 and on - had FPU
- MMX - multimedia extensions
- 57 new instructions to handle audio & video
- AMD - advanced microdevices
- AMD came in during 80486
- AMD came out with K6 (P54)
- K62 was like P55
- K63 was backward compatible
- 3DNow in later K62
- P2 had a slot that was patented
- when intel came out with slot A, AMD came out with athlon
- Athlon still had 3dNow & MMX
- 66 MHz, 100MHz intel P2
- 200 MHz FSB for Athlon
- AMD came out with double pumping
- P3 had 100MHz FSB
- P3 introed triple pipeline (TP)
- TP allowed 3 ALU's that worked at the same time
-
-
-

Pentium(r) III Processor Architectural Block Diagram



AMD Athlon™ Processor Architectural Block Diagram



4bit MPU

Worksheet 1

Machine Language	Assembly Language
A	LDA
B	ADD
C	SUB
2	JMP
3	JPZ
4	STA
5	STP
6	CMP
7	JPE
8	DIV
9	MPY

Memory Location	Contents
0	A5
1	C7
2	86
3	6A
4	7B
5	0E
6	03
7	02
8	4E
9	50
A	04
B	AD
C	28
D	0A
E	00
F	00

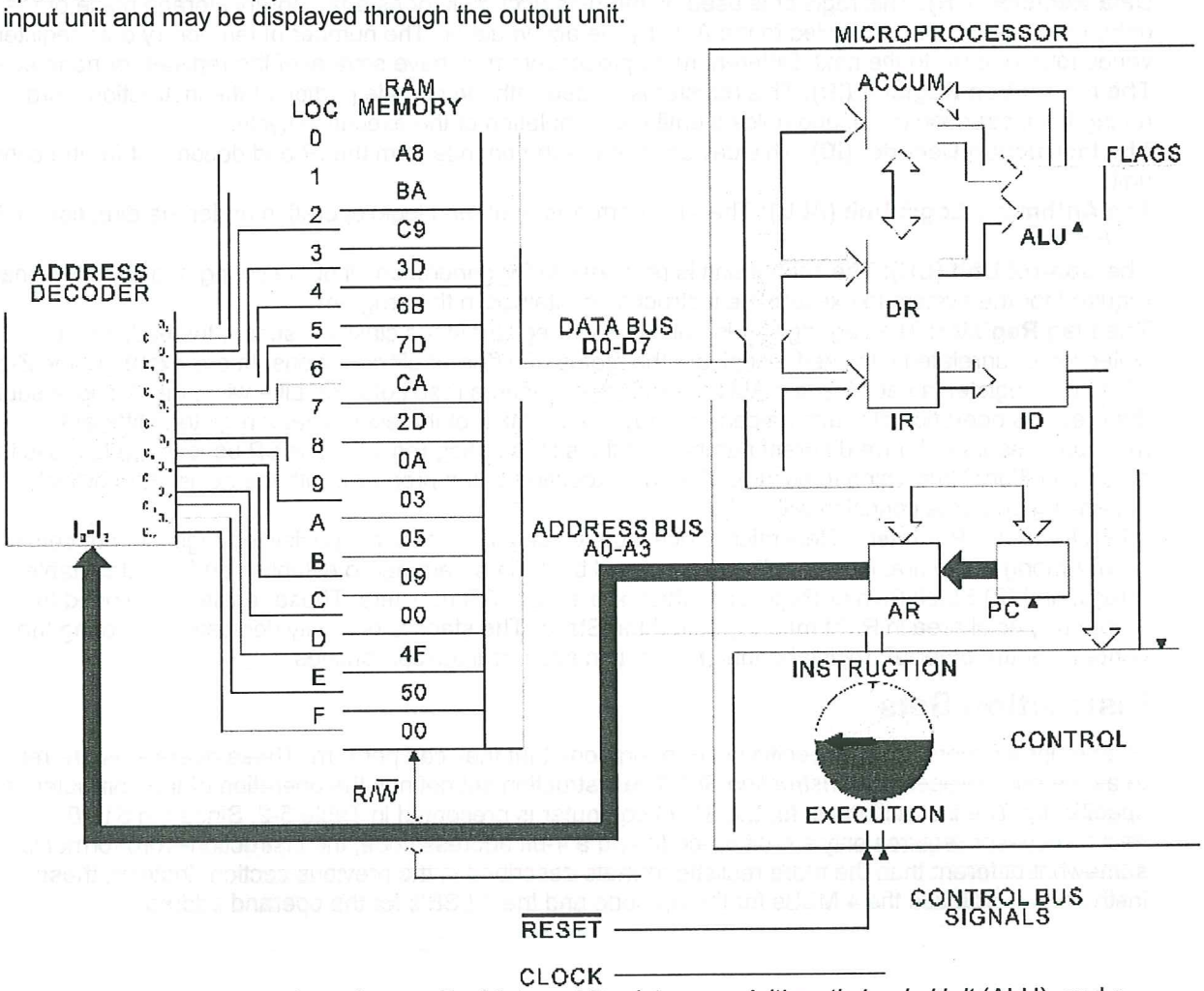
Brandon Buchanan

operand opcode

Step	Acc	DR	IR	AR	PC	Flag
1.		5	A	0	0	
	E		0	5		
2.		7	C	1	1	
	C	2	0	7		
3.		6	8	2	2	
	4	3	0	6		
4.		A	6	3	3	
		4	0	A		E-flg = 1
5.		B	7	4	4	
6.	A	D	A	B	B	
7.		8	2	C	C	
8.	E	E	4	D	8	
9.		0	5	9	9	

Microprocessor Operation

In order to better understand how a microprocessor-based system functions, let's look at a simplified computer system which we will call the $1.98 Computer. This system is based on a mythical 8-bit microprocessor which has a 4-bit address bus and is capable of performing 16 different operations. The 4-bit address bus means that this processor is only capable of addressing 16 different memory locations, but, for our applications, this should be plenty. Figure 5-7 depicts our mythical microprocessor, its internal block diagram, and a 16x8 (16 address locations and each location stores 8 bits) RAM memory block. The computer's input and output units do not actually come into play during our discussions of the system's operation. We will simply assume that our programs have been entered into the RAM memory through the input unit and may be displayed through the output unit.



The microprocessor consists of a groμP of *Internal Registers*, an *Arithmetic Logic Unit* (ALU), and a *Control Unit*. Different microprocessors will have different numbers and types of internal registers. The ones depicted here are the same as, or similar to, the registers found in nearly any microprocessor.

The Accumulator (ACCUM): This type of register is generally used by the μP to store the results of the ALU operations. It is also a source of one operand for the most ALU operations. Many μP's contain more than one accumulator register.

The Program Counter (PC): This register/counter keeps track of Instruction addresses and is always pointing at the address of the next instruction to be fetched from memory. Each time an instruction is fetched from memory, the PC is incremented by the control unit may cause the PC to jump to an address out of its normal sequential order. When the control unit received a branch instruction, such as a JUMP (JMP) or a JUMP-ON-ZERO (JPZ) command the control unit will cause the PC to be loaded with an

address portion of the instruction word. Upon execution of the jump instruction, the PC will continue its normal sequential count, beginning at the new address.
In our example, the PC is automatically reset to a value of 0. This corresponds to the beginning of our program. In real computers, the program counter is reset to some predetermined value, such as a memory location in ROM memory containing the monitor program. This location is referred to as the µP's vector address and is determined by the manufacturer of the microprocessor.
The Address Register (AR): This register is used to hold the address currently being accessed by the µP. The AR can be loaded from two different places, depending upon which part of the computer cycle is in progress. During an instruction cycle, the contents of the PC is loaded into the AR. Throughout the execution cycle, the AR is used to hold the address specified by the operand address portion of the instruction word.
Data Register (DR): This register is used by the µP's accumulator as a temporary storage place of the data. Its contents can be applied to the ALU by the accumulator. The number of temporary data registers varies form one µP to the next. Different microprocessors may have several of the register, or none at all.
The Instruction Register (IR): This register is loaded with the opcode portion of the instruction word during the instruction cycle, and holds it until the completion of the execution cycle.
The Instruction Decoder (ID): This device receives the opcode form the IR and decodes it for the control unit.
The Arithmetic Logic Unit (ALU): The ALU performs math and logic operation under the direction of the control unit.
The Control Unit (CU): The control unit is responsible for generation all of the timing and control signals required for the system to execute the instruction contained in the program.
The Flag Register: The flag register is not exactly a register in the classical sense. Instead, it is a collection of unrelated bits used to indicate the status of different µP conditions. In our example, the Z-bit of the flag register is set if the last ALU operation produced a result of zero. Like wise, the C-flag is set if the previous operation produced a carry bit beyond the MSB of the accumulator register. Different microprocessors will have different numbers of flags in their flag register. The µP uses these flag bits to allow conditional branching to occur during the execution of the program, with the decision to branch depending on some condition within the µP.
Miscellaneous Registers: Real microprocessors contain a number of specialized registers not covered here. Among these are: (1) Index Registers, used by the programmer to establish and maintain tables and arrays, and (2) Stack Pointer Registers, which are special AR registers. These registers are used to create a special area in RAM memory called the Stack. The stack is normally dedicated to storing the contents of the other µP registers during operation such as interrupt routines.

Instruction Sets

All microprocessors have a specific set of operations that they can perform. These operations are referred to as the microprocessor's *Instruction Set*. The instruction set defines the operation of the computer very specifically. The instruction set for the $1.98 computer is presented in Table 5-2. Since the $1.98 microprocessor requires only a 4-bit op-code and a 4-bit address code, the instruction-word format is somewhat different than the more realistic formats described in the previous section. Instead, these instruction words use the 4 MSBs for the op-code and the 4 LSB's for the operand address.

ASSEMBLY LANGUAGE (MNEMONIC)	MACHINE LANGUAGE HEX	BINARY	OPERATION DESCRIPTION
LDA	A	1010	Transfer the contents of the memory location specified by the operand address to the accumulator register.
ADD	B	1011	Add the contents of the memory location specified by the operand address to the contents of the accumulator, and store the results in the accumulator register.
SUB	C	1100	Subtract the contents of the memory location specified by the operand address from the contents of the accumulator, and store the results in the accumulator register.
JMP	2	0010	Jump unconditionally to the address specified by the operand address. After the jump has been executed, the instructions are taken in order from the new address.
JPZ	3	0011	Jump to the address called for by the operand address, but only if the ZERO flag is set.
STA	4	0100	Store the contents of the accumulator in the memory location specified by the operand address.
STP	5	0101	STOP; halt all operations.
CMP	6	0110	Compare the contents of the memory location specified by the operand address to the contents of the accumulator. If the two are equal, the E-flag is set.
JPE	7	0111	Jump to the address specified by the operand address, if the E-flag was set by the previous operation.

Program Execution

Referring once again to Figure 5-7, examine the hexadecimal program that has been entered into the memory. By referring to the instruction set above, we can interpret the program as described in Table 5-3.

MEMORY LOCATION	LOCATION CONTENTS	OPERATION DESCRIPTION
0	A8	LDA with contents of location 8
1	BA	ADD contents of location A to value in ACCUM and Store result in the accumulator register
2	C9	SUB contents of location 9 from value in ACCUM and Store result in the accumulator register
3	3D	JUMP to location D if ACCUM=0
4	6B	CMP the contents of location B to the value in the ACCUM, set E-flag if equal
5	7D	JUMP to location D if the E-flag is set
6	CA	SUB contents of location A from value in accumulator and store in the accumulator register
7	2D	JUMP to location D unconditionally
8	0A	DATA
9	03	DATA
A	05	DATA
B	09	DATA
C	00	DATA
D	4F	STA the contents of the ACCUM in location F
E	50	STP all operation
F	00	DATA

Brandon Buchanan

4bit MPU Worksheet 2

Note: if division does not give an integer, truncate the remainder.

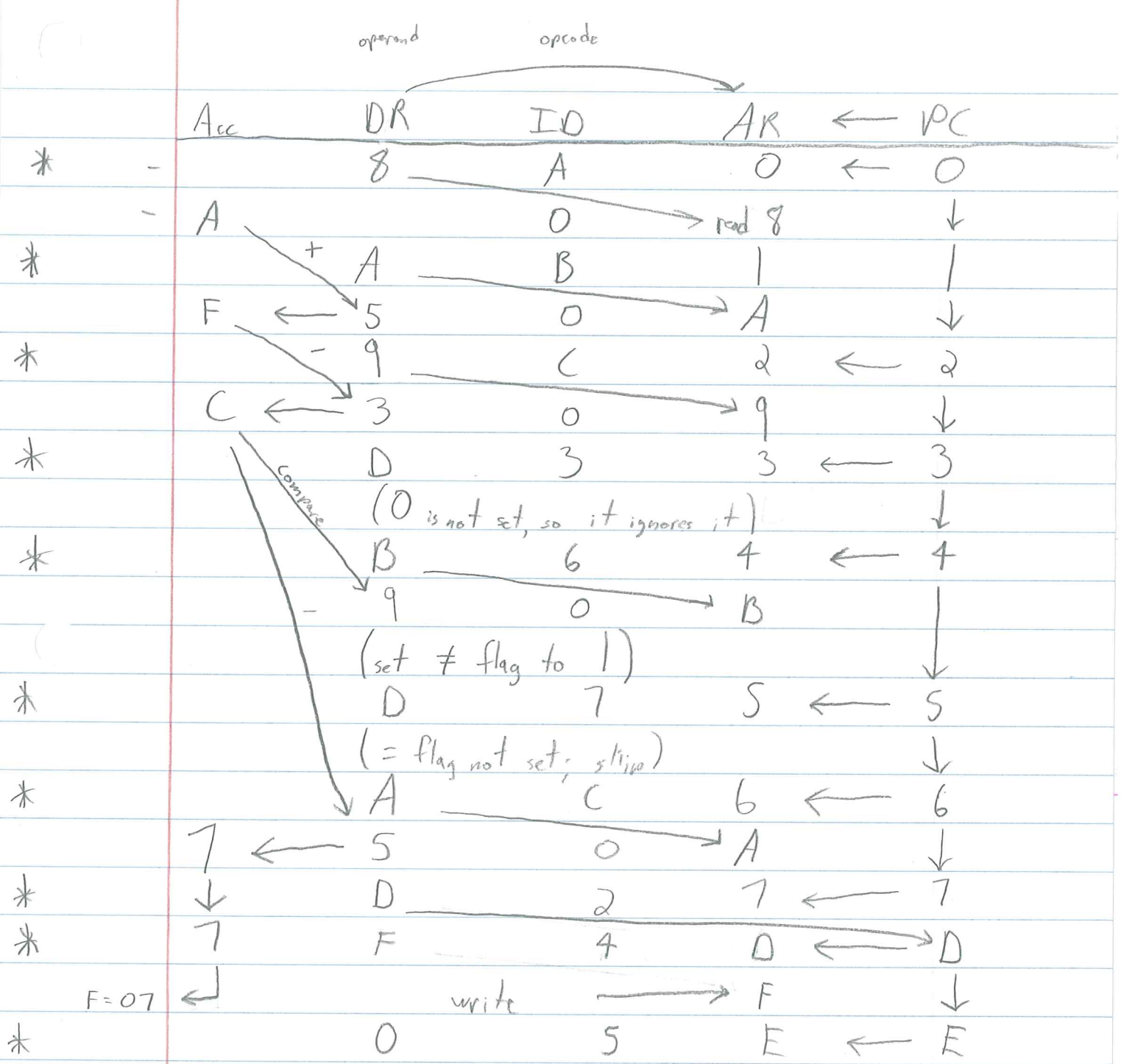
Machine Language	Assembly Language
A	LDA
B	ADD
C	SUB
2	JMP
3	JPZ
4	STA
5	STP
6	CMP
7	JPE
8	DIV
9	MPY

Memory Location	Contents
0	A8
1	9A
2	8D
3	67
4	7B
5	AF
6	21
7	02
8	03
9	50
A	03
B	4E
C	29
D	06
E	~~28~~ 02
F	04

Step	Acc	DR	IR	AR	PC	Flag
		8	A	0	0	
	3		0	8		
		A	9	1	1	
	9	3	0	A		
		D	8	2	2	
	1	6	0	D		
		7	6	3	3	
		2	0	7		
		B	7	4	4	
		E	A	5	5	
	4		0	E		
		1	2	6	6	
		A	9	1	1	
		3	0	8		

C	3	0	9		
	D	8	2	2	
2	6	0	D		
	7	6	3	3	
	2	0	7		E-flag = set
	B	7	4	4	
	E	4	B	B	E = 22
	9	2	C	C	
	0	5	9	9	Stop

* = new instruction



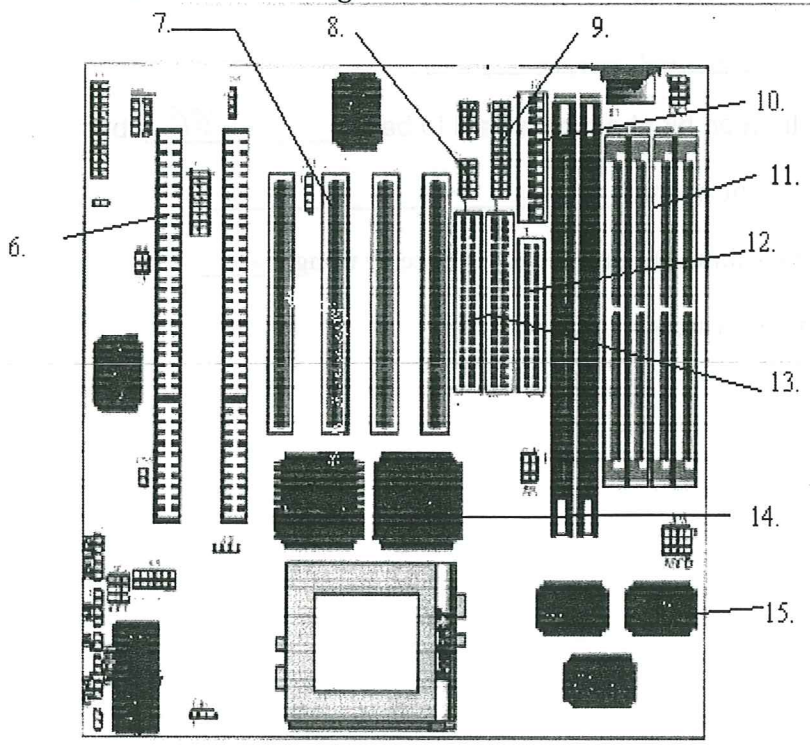
Computer Tech I **Quiz Mthrbd and Buses** **Name** Brandon Buchanan

87

3 pts each answer

1. Buses defined by their connection are called logical buses.
2. Buses defined by their function are called physical buses.
3. What is the speed of the AGP bus? 66 MHz
4. What is the bandwidth of AGPx2? (133 MHz) 266 MB/s
5. How many bits wide is the EISA bus? 16 bits

Match the number on the diagram to the answers below



6. F
7. G
8. E
9. P
10. D
11. H
12. A
13. B
14. M
15. N

Labels for the above Figure-- A. Floppy Connector B.IDE Connector C. Cache Mem. D. Power E. Com Port F. ISA Slots G. PCI Slots H. Simms mem. I. Chip Set Controller J. BIOS K. Socket 7 L. I/O Controller M. PCI-ISA Bridge N. Memory Buffers - P. parallel port

16. What is the multiplier for a 200MHz CPU on a 66MHz bus? 3x
17. What contains the basic instructions to boot up a computer? BIOS
18. Fast access memory on the motherboard (used by the CPU) is called? cache
19. Which chip of the chipset is wired directly to the CPU? memory
20. Name the bus that connects the processor to the north bridge?(logical) CPU bus

21. What is the default clock rate for the PCI bus? 33 MHz ✓

22. What is the default clock rate for the ISA bus? 33 MHz ✓ 1

23. Name the four "physical bus groups"

a. I/O bus ✓ 1

b. controller bus

c. speed bus ✓ 1

d. carrier bus ✓ 1 ✓ 1

24. What is the max. bandwidth for 16 bit ISA? 66 MB/s

25. For what does AGP stand? accelerated graphics port

26. A bus which transfers more than on bit at a time is said to be a "parallel" bus

27. USB transfers how many bits at a time? 1 bit

28. Setting the motherboard to operate with various processors is done by using jumpers.

29. What 2 things must you set for all processors?

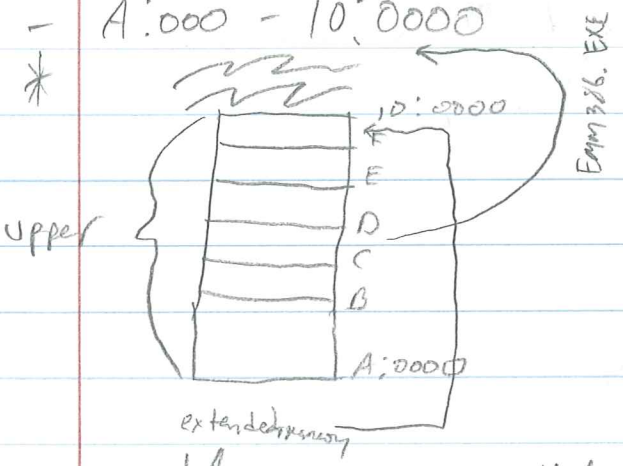
a. voltages

b clock speed

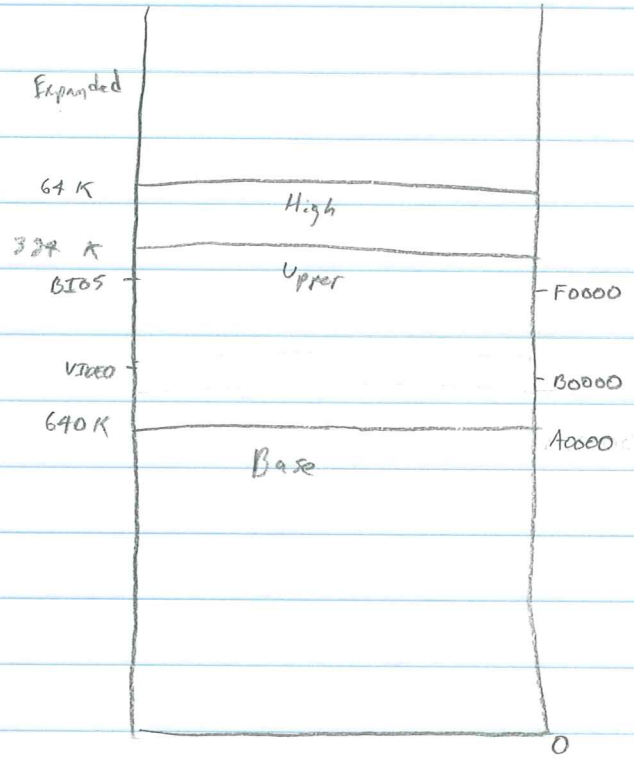
Memory

* * Logical
  - real mode - DOS — 1 MB of memory
  - protected mode - 1+ MB of memory
* * Real Mode
  - goes from 0 - FFFFF
  - conventional memory
  - 0-9FFFF - base memory
  - upper
  - 8086 uses offset addresses
  - each segment is 64K
  - 20-bit bus adds two memory
  - 80000 is reserved for video
  - Bottom is video graphics
  - top is monotext
  - 3C1A
  - under 1 Meg is conventional memory
  - base memory - 640K
  - upper memory - after 640K
  - A:0000 - C:0000 is for video card
  - F:0000 - F:FFFF - PS/2 BIOS
  -

- extra devices - extra 64K
- A:000 - 10:0000
- *



- expanded memory - memory that switches into
- EMS - expanded memory system
- XMS - extended "
- 0:0000 - 0:0400 - I/O - vector area



himem.sys - access
him mem

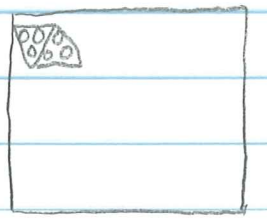
emm386.exe - access
expanded

- protected - over 1 MB or Non-DOS systems
- real - under 1 MB
- imem.sys
- high memory area - logical in real mode & not extended mem.
- high memory is above 1 MB
- it exist because of a mistake
- real mode - expanded memory can maybe exist
- it exists if XMS emm386.exe is there
- upper memory is 384K A:0000 - F:0000
- 2 spots reserved for video & BIOS
- other spots are device drivers & page frames into expanded memory (the switching) & adapter ROM
- video RAM can read/write at same time
- bank is how many you need to make it work as 64-bit
-

* * Physical Bus Packaging
- SIPP - single inline plastic package > individual chips
- DIPP - dual " "
- SIMM - single inline memory module - 30 pin & 72 pin
- DIMM - dual
- SODIMM - laptop

* * Stuff
- static RAM - memory stays there and available all of the time
- dynamic RAM - must be refreshed (read and write)
- DRAM - ↗
- SDRAM - synchronous DRAM
- FPM - fast page mode, assumed that the memory address was the next location
- EDO - extended data out, one step further in FPM, slow machines
- BEDO - burst EDO
- RDRAM - Intel only
- Rambus DRAM - ↗
- DDRDRAM - double data rate " - read data &
- DCDDR - dual channel "

Video



line by line - non interlaced
a TV skips lines - interlaced

- each line is composed of dots
- only 3 colored dots - red, green, blue
- red + green → yellow
- red + blue → magneta
- blue + green → cyan
- triad is a R, G, B
- 

that square is 1 color
- smallest piece of display w/ same properties is a pixel
- resolution is the pixels in a row by a row
- 1 frame is a complete drawing of the screen
- vert. refresh - the refresh rate

---

* * video standard - based on resolution + colors
* MDA - monochrome display adapt
- displays 80 characters wide by 25 deep
- 720 x 350 graphics (1 color)

* CGA - color graphics adapt
640 x 350 in 16 colors
80 chars. x 25 chars.

* VGA - video graphics adapt
640 x 480 in 16 colors B:8000 - B:FFFF

* Enhanced Graphics Adapt.
- 16 colors
- 640 x 350
* VGA
- 640 x 980 x 16 colors
- 80 x 25 characters
* XGA - Extended Graphics Adapt.
- 1024 x 768 in 256 colors
* SXGA - Hyper "
- 1280 x 1024 in 256 colors
* UXGA - Ultra "
- 1600 x 1200 in 256 colors
* SVGA - no standard - Hyper "
- 800 x 600 or 1024 x 768
* * Color
- 1 bit - monochrome
- 2 bit - 4 colors
- 4 bit - 16 colors
- 8 bit - 256 colors
- 16 bit - 65536 colors high color (XP-medium)
- 24 bit - 16,777,216 colors true color
- 32 bit - 4,294,967,296 colors

- anti-alias - smooth transition at edge
- dithering - colors from a smaller set
- textures - displaying a pixel as one of a standard set of textures
- perspective - adjusting size to give illusion of depth
- focus - far objects lose clarity
- blurring - technique to simulate speed
- Z-buffering - keeps track of what is in the foreground and background
-

Storage Devices

* * SCSI
- small computer system interface
- a card where controller can handle up to 15 devices (7 internal / 7 external)
- done in a daisy chain config
- RAID - redundant array of inexpensive disks
- RAID 0 known as disk duplexing
- RAID 5 can use 3-5 disks
- RAID 5 uses disk striping
- the parody cluster keeps track of what info was above
- if a hard drive were to fail, the parody disk could rebuild the failed hard drive

* * IDE - integrated device electronics
- ATAPI - AT attach peripheral interface
- compatible with IDE using device drivers
- the driver communicates between device & OS

* * SATA - serial ATA
- faster bus than IDE

* * IDE Channel
- primary
- secondary
- 2 devices each
- boot device must be on primary channel
- 40 pin & 80 pin
- pin 1 is usually near power connector
- 2 wires per pin running at different frequencies

- jumpers can be set for master or slave or CS - cable select
- master controls the whole channel
- if slave can deal with channel, it's fine, but if slave can't, the channel might not recognize a slave
- secondary has master and slave or CS
- cable select allows OS or motherboard to control settings
- 55 AA is head 0, cylinder 0, sector 1
- 55 1A is the boot sector indicator
- floppies are not IDE or ATAPI
- each layer that the head writes to is a track
- cylinder is a group of tracks with same ##
- a track is broken up into sectors
- a HD has 64 sectors, but with index, only 63 are available
- all sectors have 512 bytes
- tracks × heads × sectors × 512 = space available

** File Allocation Table
- keeps track of where parts of disk start
- FAT 12 FAT 16 FAT 32, NTFS
- NTFS = new technology file system
- FAT12 - 4096 combos
- FAT16 - 65,536 ~~combos~~ clusters
- FAT32 - 4 billion
- a cluster is a group of sectors acting as one data unit
- smallest cluster is 512 bytes
- clusters can be in range 512 byte - 1K - 2K - 4K - 8K - 16K - 32K
- 32K cause it uses 64 sectors

- HD size in FAT 16
- find max. HD size, multiply cluster size x sectors
- 32768 x 65536 = 2 GB

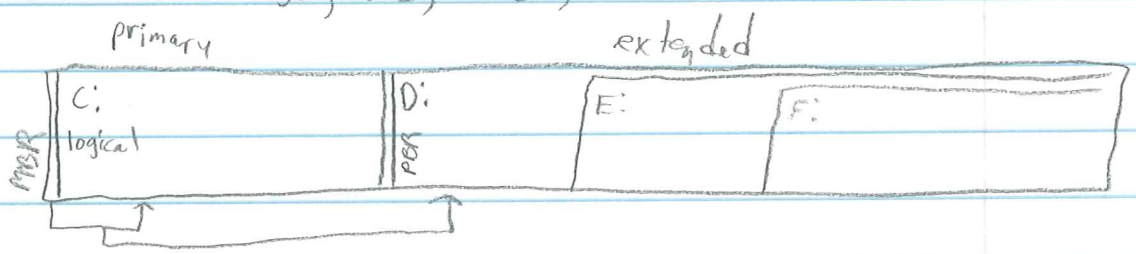
cluster size x number of clusters = space in FAT 16

** Partitioning a HD

- breaking a single physical drive into 2 or more logical drives
- primary partition
- extended partition

> FAT

- FAT can only be broken up into 2 logical drives
- at location - 1BE, 1CE, 1DE, 1EE

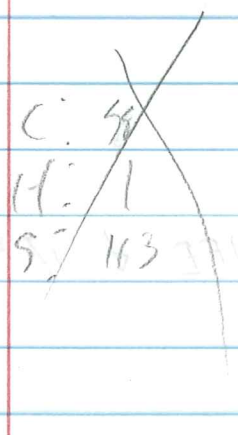


- you can have 23 logical drives
- MBR - master boot record
- cylinder 0, head 0, sector 1 is MBR
- MBR shows drives
- MBR shows which one to boot from
- D: has a partition boot record
- PBR tells where logical drives is
- E: PBR tells where F: is
- FDISK is program to partition
- FORMAT - program to prepare a disk to receive data

- A:1> - DOS prompt
- DIR - tells programs /P ac page at time
- A:1> FDISK
-

not

B	head	c/s	cylinder
1BE	1BF	1C0	1C1



not boot C: 319 H: 1 S: 99

11000000

80 01 C0 2D 32D

bootable C: 813 H: 1 S: 0

00 FF FF FF

nonbootable C: 1023 H: 255 S: 63

* * Boot Record
- IBE, ICE, IDE, IEE
- 3 infos after
- point to partitions
- to find boot records, search for 55AA ; IFE & IFF

* * Formatting
- format C:
- clears FAT 1 & 2
- clears directories (tells where first cluster is)
- FAT - tables for DOS, starts with F8 no final info
-

- slack is a waste of space
* To find cluster size

Ex - 500 MB Volume

800 K · KB

$\frac{800\ K \cdot KB}{64\ K\ cluster}$

$12.5\ \frac{KB}{cluster}$

- 16 KB cluster size

- ~~set blaster~~ (AUTOEXEC.BAT)
- set blaster = A220 I5 D1 T3 P330 E620
- last are optional I/O Addr. interrupt DMA
- ~~#5 - IDE~~
- ~~Floppy~~
- ~~sound~~
- ~~DMA~~
- #0 - system clock
- #1 - keyboard
- 2 - pass to 8-15
- 3 - COM2 or COM4
- 4 - COM1 or COM3
- 5 - secondary parallel port (found) (LPT2)
- 6 - floppy
- 7 - LPT1
- 8 - real time clock
- 9 - network cards (available) (Windows takes over for PCI)
- 10 - available
- 11 - available
- 12 - PS2 mouse
- 13 - FPU
- 14 - primary IDE
- 15 - secondary IDE (available if empty)

* # DMA channels
- 0 - system use
- 2 - floppy drive (only cache memory)
- 1 - open, but usually used for sound
- 5 - used by some sound card for stereo
- 7 total channels

* * IO address
- I/O data for addressing
- 1K addressing 000 - 3FF
- 220 is standard for sound blaster comp. cards
- 240 is alternate sound
- 200 - MIDI
- 080 - output of POST (power on self test)
- 170 - IDE secondary
- 1F0 - IDE primary
- 2F8 - COM2
- 3F8 - COM1
- 378 - parallel port
- 3C0 - printer (obsolete)
- 380 - color graphics
- 3B0 - black & white graphics

		IRQ
-	COM1 - 3F8	4
-	COM2 - 2F8	3
-	COM3 - 2F8	4
-	COM4 - 2E8	3

* * D → A Converters
- height is loudness
- width is pitch
- called FM synthesis
- original way
- DSP - digital signal processor

* * Wavetable
- has a matrix built into it
- looks up code for sound
- software wavetable - held in memory
- hardware wavetable - sounds are on chip

- each piece is a sample
- how many samples is sample rate
- with no sound database - FM synthesis
- set blaster (command)
- must be space between words (no space between blaster and =)
- DI = DMA
- MIDI - musical
- BIOS - PCI / PNP (changes for PCI/PNP)
- interrupts handled by auto or manually
-

* Modem
- placed on COM2 or COM4 usually
- works on voice line
- modulates voice frequencies as 1's & 0's
- baud rate - how fast bits/sec
- AT - attention
- DT / DP - dial tone / pulse
- H - hang up
- LAN - confined to a small geographic area
- MAN - metropolitan... size of city
- WAN - country or around the world
- STAN - star trek - covers galaxy
- modem are classified as a WAN device

- XMODEM is a protocol 5900 bits
- Y + Z are better versions of X
- ATAT - attention
- D - dial number
- P or T - pulse or tone
- ATZ - reset modem
- ATH0 - hang up
- ATH1 - pick up
- A - answer
-

Review

- L switch - assigns drive letter, works with MSCDEX.EXE
- AT & PC AT is less
- device = C:\bak\cdrom.sys /D: [name]
- IRQ - com1 = 4
- IRQ - serial 1 (com2) = 3
- serial 0 = com1 ++
- DMA for sound = 1
- DMA - MIDI - 5 (advanced sound, MIDI)
- IRQ 14 - primary
- DMA - 3 doesn't exist 0, 1, 2, 4, 5, 6, 7
- IRQ 2 is missing
- autoexec.bat to configure sound
- address for sound I/O is 220
- IRQ = 5 for sound
- IRQ available - 9, 10, 11
- floppy IRQ = 6
- PS/2 mouse IRQ - 12
- printer IRQ - 7
- I/O address = 378 - parallel 0 (LPT1)
- parallel 7, mouse 12, 0, 1, 8, 9, 10, 11, 12, 13, 14, 15, 3, 4, 5, 6, 7
- floppy DMA = IRQ 6, DMA 2
- two IRQ to serial mouse = 3 & 4
- wavetable
- hardware wt is in chip or card

Printers

* Six Steps
- cleaning - residual toner is scraped from the drum
- conditioning - negative charge placed on drum
- writing - laser beam strikes the drum to form latent image (L.I.)
- developing - the L.I. is developed by placing toner on paper
- transferring - dev. image trans. to paper
- fusing - when toner melts to paper

* Other
- period can be used but will degrade the performance
- EP = electrophotostatic

* Printer Types
- impact - forms images by striking a ribbon by pressing it against the paper
- non-impact - uses lasers or magnets or high heat
- impact examples - daisywheel, thimble, letter-quality, printers, dot matrix
- dot matrix printers use 9, 18, 24
-

* * Impact
- letter - dot matrix 7, 9, 18, & 24 pins NLQ (near letter quality)
- fully formed - daisy wheel, thimble
* * Thermal
- special paper is heated
* * Ink
- inkjet - piezoelectric crystal - runs a current and it squeezes ink
- bubblejet - boil ink
* * Specialty Printers
- Hotwax -
* * Lasers
- ((WDTF
* * Paper
- wt or grammage (basis) pounds, grams
- caliper - thickness inch
- finish - gloss or not (smoothness) sheffields or bekks (sh: 350 per dlkr)
- grain curl - mx rules to measure (warp)

* * Topology
- physical - how cable up
- logical - the way it functions
* Physical
- bus topology - device connected by 1 wire
- CSMA/CD - Ethernet
- carrier sense multiple axio / collision detection
* Ring
- computer connected to each computer
- also known as token ring
* Double Ring
- MAU - media attachment unit
- FDDI - fiber distributed data infrastructure
* Mesh
- everything connected to each other
- $\frac{n(n-1)}{2}$
* Protocol
- set of rules for communication
* * OSI Model
- breaks communication down into 7 layers
7. - application
6. - presentation
5. - session
4. - transport
3. - network
2. - data link 1. physical layer

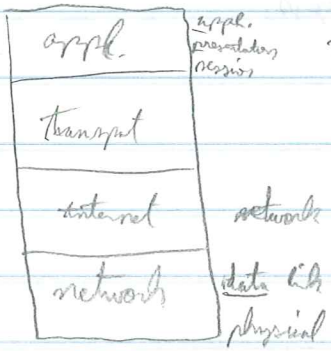
- physical layers must talk directly with another machine's physical layer

host to host communications
- physical — bits, wires →
- data link — physical addressing, framing of data →
- network — logical addressing, packet, path selection →
- transport — reliability, segment →

application to application
- session — sets up, tears down →
- presentation — JPEG, GIF, ASCII →
- application — FTP, HTTP, Telnet →

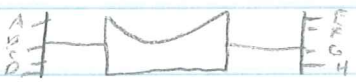
- data → encode → data stream
- then stream is broken into pieces
- a header is placed on each piece
- header tells how much data, order, ~~[illegible]~~, etc...
- segments has logical addressing on front
- packet expands all this
- physical addressing is on both front and checksum on back
- frame is all there
- frame is then sent once converted to bits

- TCP/IP model



* * Layer 1 - Physical
- cabling
- repeaters
- hubs
- transceivers
- in 10base2, 185 meters long or "200" - thinnet
- in 10base5, 500 meters long - thicknet
- 10baseT - 100 meters
- 100baseT - 100 meters
- 10 or 100 is digital bandwidth in Mbps
- base is for baseband
- baseband is data on one wire
- broadband carries more than one signal
- T is twisted pair cabling
- TX is extension of T
- 100baseFX - F is for fiber

* * Layer 2 - Data Link
- framing, physical addressing
- NIC - network interface connector
- physical address - 6 bytes long
- XX XX XX XX XX XX
- first three are manufactuer code
- last three are serial number
- bridge is a level 2 device



- switch

* Layer 3 - Network layer

- routers

- MAC address FF-FF-FF-FF-FF-FF is a broadcast
- ip address - 192.168.1.15 - identifies network
- transport address - port/socket
* * IP Networking addressing
- * classful addressing
* Class A
- N.H.H.H
- N is network number
- H is host
- first byte starts with a 0 $0_{xxx\ xxxx}$
- range of 0-127
- 128 networks
* Class B
- N.N.H.H
- 64K hosts max
- first byte starts at $10_{xx\ xxxx}$
- range of 128 - 191
- 16K possible networks
* Class C
- N.N.N.H
- first byte at 110_{x} xxxx
- range 192 - 223
* Class D
- first byte 1110 xxxx
- range 224 - 239
* Class E - Research
- 1111 xxxx - 240 - 255

reserved

bvtlsdj

- 192.168.1.0 - network address
- 192.168.1.1 - 192.168.1.255 ← broadcast
- 10.0.0.0 + Subnet Mask
- normal subnet mask in A is 255.0.0.0
- (lass B - 255.255.00
- (- 255.255.255.0

- collision domain - area where two signals can collide
- broadcast domain - all devices that a comm can broadcast to
- IDF - intermediate distribution facility
- MDF - main DF
- rollover, crossover, patch cables
- 568A 568B
- 568A done by Xerox
- 568B is most common
- 568A - 8 pins
- 568B - 8 pins

	1	2	3	4	5	6	7	8
568A	G/w	G	O	B	B/w	O/w	B/w	B
568B	O/w	O	G/w	B	B/w	G	B/w	B

- O/w is the transmit +
- O is transmit ground
- G/w receive +
- G is receive ground

(568B)

- pins 1, 2, 3, 6 are receive/transmit pins
- rollover cable goes 1, 2, 3.. on one side and 8, 7, 6...
- used always for serial communications

- set of rules - protocol
- easy to troubleshoot & helps to design for models (TCP/IP or other layers)
- OSI - connectivity is in layer 3 (network)
- reliable network communication in layer 4 (transport)
- presentation layer encrypts & data formatting
- data link layer - physical addressing & framing & topology
- physical - bits & wires
- transmission media is in physical
- process of controlling data (russian dolls) is encapsulation
- encapsulation includes information on both (front is header, end is trailer)
- steps for encaps.
- segments → packet → frame → bits
- flow control is in the transport layer
- frames are created in data link layer
- packets are created in layer 3
- fiber optic - signal length & not affected by noise
- horizontal - to end host
- vertical -
- patch - patch panels
- work area - comp / work area
- inverted is a rollover cable
- crossover are one comp to comp
- patch goes X without X (straight through cable)
- twist wires to cancel noise
- collision is when 2 comps talk at same time
- network has 3 hubs - no collisions

- network with 3 switches has 3 collision domains
- broadcast domain will be 1
- routers break up broadcast domain
- breaking up collision domain is segmentation
- bus topology is when everything on one wire
- star is connected at central point
- extended has different branches of stars
- class C address has 3 network bytes (N.N.N.H)
- 1's tells network is what each, 0's is host
- CAT5 uses RJ-45
- mail & file transfer are application layers
- encoding moves into presentation layer
- IP uses 4 layers that correspond (1,2 network, 3 internet,)
- IP works at layer 3, TCP at layer 4
- 3 way handshake - sets up error correction
- TCP is reliable, UDP isn't
- 10baseT uses 1,2,3,6 wires
- max length for 10base2 is 185
- 10base2 uses BNC
- 8 pins in RJ-45
- only uses 8 is gigabit
- TCP/IP needed for internet
- NIC with 8 and 7 pins is fiber ring
- 0-127 for Class A network
- layer 2 protocol Net Bueui
- ~~peripheral~~ parallel doesn't need DMA ~~for internet~~ to work