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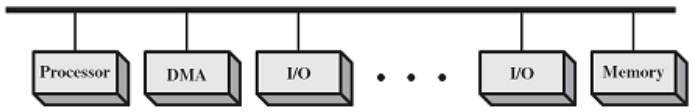
**Correct**

**Q.1)** In a single error correction system, if the stored data and parity bits had a single bit error in one of the parity bits, the binary representation of the syndrome word would be made from _____.

**A.** all ones
**B.** all zeros
**C.** exactly one one and the rest zeros (Your Answer)
**D.** two or more ones with the possibility of all ones
**E.** cannot be determined

**Correct**

**Q.2)**




**Single-bus, detached DMA**

In a configuration like the one shown above where the DMA controller, the I/O device supported by the DMA, and the memory share a single bus with the CPU, the DMA requires _____ access(es) to the bus to transfer a single word from the I/O device to memory.

**A.** 1
**B.** 2 (Your Answer)
**C.** 3
**D.** Cannot be predicted

**Correct**

**Q.3)** In a single error correction system, if the stored data and parity bits had a single bit error in one of the data bits, the binary representation of the syndrome word would be made from _____.

**A.** all ones
**B.** all zeros
**C.** exactly one one and the rest zeros
**D.** two or more ones with the possibility of all ones (Your Answer)
**E.** cannot be determined

**Correct**

**Q.4)** Which of the following I/O methods requires the CPU to check the I/O device regularly to see if it needs attention? Select all that apply.

**A.** programmed I/O (Your Answer)

**B.** interrupt driven I/O
**C.** direct memory access

**Correct**

**Q.5)**

| Bit ID | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| ID in binary | 1111 | 1110 | 1101 | 1100 | 1011 | 1010 | 1001 | 1000 | 0111 | 0110 | 0101 | 0100 | 0011 | 0010 | 0001 |
| Data bit | Not used | Not used | Not used | $D_7$ | $D_6$ | $D_5$ | $D_4$ | | $D_3$ | $D_2$ | $D_1$ | | $D_0$ | | |
| Check code bit | | | | | | | | $P_3$ | | | | $P_2$ | | $P_1$ | $P_0$ |

***For the next four questions, use the diagram shown above that describes the assigned syndrome values corresponding to eight data bits ($D_0$ through $D_7$) and four parity bits ($P_0$ through $P_3$).***

The parity bits are computed by taking the exclusive-OR of different combinations of data bits. From the list below, select ***ALL*** of the data bits that would be exclusive-OR'ed together to create the parity bit P2.

**A.** D0
**B.** D1 (Your Answer)
**C.** D2 (Your Answer)
**D.** D3 (Your Answer)
**E.** D4
**F.** D5
**G.** D6
**H.** D7 (Your Answer)

**Correct**

**Q.6)** What is the solution to storing global variables?

**A.** to assign symbolic or virtual register destination
**B.** to create a global pointer for referencing purposes (Your Answer)
**C.** to reduce the number of registers
**D.** to create an additional set of registers (Your Answer)

**Correct**

**Q.7)** The processor checks for interrupts _____. Select the best answer.

**A.** at all times during the execution of a machine-level instruction
**B.** only when the application executes a software interrupt
**C.** during each read or write access to the system bus
**D.** at the end of the execution of a machine-level instruction (Your Answer)

**Correct**

**Q.8)** A system bus error generates a(n) _____.

**A.** software interrupt
**B.** maskable hardware interrupt
**C.** non-maskable hardware interrupt (Your Answer)
**D.** exception

**Correct**

**Q.9)** How many parity bits would be needed to develop a single error correction scheme (with NO double error detection) for 48 data bits?

**A.** 5
**B.** 6 (Your Answer)
**C.** 7
**D.** 8
**E.** 9

**F.** 10

**Correct**

**Q.10)**

| Page # | |
|---|---|
| 1FA | 4CA |
| 1FB | CA1 |
| 1FC | 37E |
| 1FD | 4B3 |
| 1FE | D04 |
| 1FF | 3E1 |
| 200 | 715 |
| 201 | 716 |

The next 2 problems are based on the figure above representing a ***portion*** of a page table for a process on a system that allocates $2^{24}$ = 16 Meg worth of memory space to a process. Note that the page numbers shown do not start at 0, but the ***whole*** page table itself does!

Calculate the physical address from the logical address $1FECD0_{16}$ (shown in hexadecimal). Assume a page size of $2^{12}$ = 4K words. The page numbers and the values in the page table are in hexadecimal.

**A.** 1FED04v16
**B.** 1FECD0v16
**C.** D043E1v16
**D.** CD0D04v16
**E.** D04CD0v16 (Your Answer)
**F.** The portion of the page table shown doesn't allow for the answer to be determined.

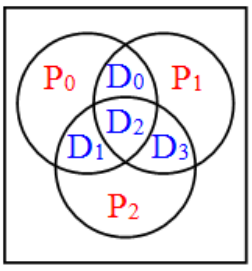
**Correct**

**Q.11)** Which type(s) of interrupt configurations are easily expandable to greater numbers of devices regardless of their interface to the CPU? Select all that apply.

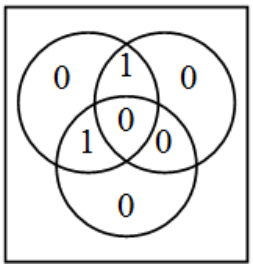
**A.** Separate interrupt pins for each device
**B.** Daisy chain/hardware poll (Your Answer)
**C.** Software poll (Your Answer)
**D.** Bus arbitration (Your Answer)

**Correct**

**Q.12)**




***For the next question, use the diagram shown above to identify the bit names ($D_0$, $D_1$, $D_2$, $D_3$, $P_0$, $P_1$, and $P_2$) of a 4-bit Hamming code by their position in the figure.***




Assume the graphic above depicts the data and parity digits of a 4-bit Hamming code. Assuming there is a single bit error, which bit flipped?

**A.** D0
**B.** D1
**C.** D2
**D.** D3 (Your Answer)
**E.** P0
**F.** P1
**G.** P2

**Incorrect**

**Q.13)** Of the following types of interrupts, which are asynchronous, i.e., cannot predict when they will happen? Select all that apply.

**A.** software interrupts (Your Answer)
**B.** hardware interrupts (Correct Answer)
**C.** exceptions

**Correct**

**Q.14)** True/False: Only a single "global" parity bit needs to be added to a single-error correction scheme in order to add double-error detection capabilities regardless of the number of data bits.

**A.** True (Your Answer)
**B.** False

**Correct**

**Q.15)**

| Bit ID | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| ID in binary | 1111 | 1110 | 1101 | 1100 | 1011 | 1010 | 1001 | 1000 | 0111 | 0110 | 0101 | 0100 | 0011 | 0010 | 0001 |
| Data bit | Not used | Not used | Not used | $D_7$ | $D_6$ | $D_5$ | $D_4$ | | $D_3$ | $D_2$ | $D_1$ | | $D_0$ | | |
| Check code bit | | | | | | | | $P_3$ | | | | $P_2$ | | $P_1$ | $P_0$ |

***For the next four questions, use the diagram shown above that describes the assigned syndrome values corresponding to eight data bits ($D_0$ through $D_7$) and four parity bits ($P_0$ through $P_3$).***

For the error correcting system of the previous question, assume that the check code ***retrieved*** from memory was $P_3 = 0$, $P_2 = 0$, $P_1 = 0$, $P_0 = 1$, and the newly ***calculated*** check code on the data retrieved from memory was $P_3 = 0$, $P_2 = 1$, $P_1 = 0$, $P_0 = 0$. Assuming a single bit error has occurred, which bit was the one that flipped, $D_7$, $D_6$, $D_5$, $D_4$, $D_3$, $D_2$, $D_1$, $D_0$, $P_3$, $P_2$, $P_1$, or $P_0$?

**A.** D0

**B.** D1 (Your Answer)
**C.** D2
**D.** D3
**E.** D4
**F.** D5
**G.** D6
**H.** D7
**I.** P0
**J.** P1
**K.** P2
**L.** P3

**Correct**

**Q.16)** Which of the following I/O methods allows for the simplest/least intelligent of I/O devices? Select only one.

**A.** programmed I/O (Your Answer)
**B.** interrupt-driven I/O
**C.** direct memory access

**Incorrect**

**Q.17)** Which of the following are possible causes of thrashing? Select all that apply.

**A.** Working set is too large for installed memory. (Missed)
**B.** Program doesn't exhibit locality of reference. (Your Answer)
**C.** Cannot fit all of the pages from the application/process into available memory.
**D.** Too many processes running at the same time. (Your Answer)

**Correct**

**Q.18)** Which of the following I/O methods requires the CPU to be capable of using interrupts? Check all that apply.

**A.** programmed I/O
**B.** interrupt-driven I/O (Your Answer)
**C.** direct memory access (Your Answer)

**Correct**

**Q.19)** . Which of the following I/O methods requires the least amount of CPU intervention? Select one.

**A.** programmed I/O
**B.** interrupt driven I/O
**C.** direct memory access (Your Answer)

**Correct**

**Q.20)**

| Bit ID | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| ID in binary | 1111 | 1110 | 1101 | 1100 | 1011 | 1010 | 1001 | 1000 | 0111 | 0110 | 0101 | 0100 | 0011 | 0010 | 0001 |
| Data bit | Not used | Not used | Not used | $D_7$ | $D_6$ | $D_5$ | $D_4$ | | $D_3$ | $D_2$ | $D_1$ | | $D_0$ | | |
| Check code bit | | | | | | | | $P_3$ | | | | $P_2$ | | $P_1$ | $P_0$ |

***For the next four questions, use the diagram shown above that describes the assigned syndrome values corresponding to eight data bits ($D_0$ through $D_7$) and four parity bits ($P_0$ through $P_3$).***

For the error correcting system of the previous question, assume that the check code ***retrieved*** from memory was $P_3 = 1$, $P_2 = 1$, $P_1 = 0$, $P_0 = 1$, and the newly ***calculated*** check code on the data retrieved from memory was $P_3 = 0$, $P_2 = 0$, $P_1 = 1$, $P_0 = 1$. Which of the following descriptions best describes what has happened?

**A.** There is no error in the data or parity bits

**B.** There is a single bit error.
**C.** There are multiple bit errors. (Your Answer)
**D.** It is impossible for this situation to occur

**Correct**

**Q.21)** Identify some of the problems with reducing the semantic gap:

**A.** inefficient execution of code (Your Answer)
**B.** simplified compilers
**C.** excessive machine code instruction size (Your Answer)
**D.** increased complexity of compilers (Your Answer)
**E.** many compiler writers found it too hard to implement complex instructions (Your Answer)

**Correct**

**Q.22)** In a single error correction system, if the stored data and/or parity bits had multiple bit errors, the binary representation of the syndrome word would be made from _____.

**A.** all ones
**B.** all zeros
**C.** exactly one one and the rest zeros
**D.** two or more ones with the possibility of all ones
**E.** cannot be determined (Your Answer)

**Correct**

**Q.23)** The _____ is a one-to-one mapping of physical frames existing in physical memory to the application's pages that are contained in them.

**A.** inverted page table (Your Answer)
**B.** translation lookaside buffer

**Correct**

**Q.24)** The _____ potentially solves the problem of very large page tables taking up too much space in memory.

**A.** inverted page table (Your Answer)
**B.** translation lookaside buffer

**Correct**

**Q.25)**

| Page # | |
|---|---|
| 1FA | 4CA |
| 1FB | CA1 |
| 1FC | 37E |
| 1FD | 4B3 |
| 1FE | D04 |
| 1FF | 3E1 |
| 200 | 715 |
| 201 | 716 |

The next 2 problems are based on the figure above representing a ***portion*** of a page table for a process on a system that allocates $2^{24}$ = 16 Meg worth of memory space to a process. Note that the page numbers shown do not start at 0, but the ***whole*** page table itself does!

For the previous problem ($1FECD0_{16}$), what is the logical address' offset into the page?

**A.** CD0v16 (Your Answer)
**B.** 1FEv16
**C.** D04v16
**D.** 1FECD0v16
**E.** D04CD0v16
**F.** The portion of the page table shown doesn't allow for the answer to be determined.

**Correct**

**Q.26)** Which of the following statements is true about DMA cycle stealing?

- **A.** The CPU is suspended for a bus cycle (either read or write) so that the DMA can transfer a word of data. (Your Answer)
- **B.** The DMA interrupts the CPU in order to access the system bus for a transfer.
- **C.** A cache may reduce some of the effect of cycle stealing by allowing CPU to execute code without accessing the system bus. (Your Answer)

**Correct**

**Q.27)** Which term below identifies the component of the interrupt system that identifies the address of the interrupt service routine (ISR)?

- **A.** interrupt vector (Your Answer)
- **B.** local interrupt enable
- **C.** interrupt mask
- **D.** interrupt flag

**Incorrect**

**Q.28)** Which of the following statements are true when writing an ISR in a high-level language such as C++?

- **A.** The ISR declaration is much like a method declaration with both the parameters and return value typically set to “void”, i.e., you do not pass variables to or return a value from an ISR. (Correct Answer)(Your Answer)
- **B.** If the system already has an ISR declared for this particular interrupt, you cannot replace it with your own ISR.
- **C.** Since high-level languages use variables from memory, the system context does not need to be saved or restored. (Your Answer)
- **D.** None of these statements are true. ISRs must be written in assembly or machine language.

**Correct**

**Q.29)** A divide by zero error generates a(n) _____.

- **A.** software interrupt
- **B.** maskable hardware interrupt
- **C.** non-maskable hardware interrupt
- **D.** exception (Your Answer)

**Correct**

**Q.30)** Which term below identifies the component of the interrupt system that serves to identify which interrupts have been triggered?

- **A.** interrupt vector
- **B.** local interrupt enable
- **C.** interrupt mask
- **D.** interrupt flag (Your Answer)

**Correct**

**Q.31)** Of the following types of interrupts, which always occur at the same location in code regardless of the processor state or data conditions?

- **A.** software interrupts (Your Answer)
- **B.** hardware interrupts
- **C.** exceptions

**Correct**

**Q.32)** When a DMA has completed its transfer, it generates a(n) _____.

- **A.** software interrupt
- **B.** maskable hardware interrupt (Your Answer)
- **C.** non-maskable hardware interrupt
- **D.** exception

**Correct**

**Q.33)** A RISC processor has ...check all that apply

- **A.** Optimized pipeline (Your Answer)
- **B.** Limited/simple instruction set (Your Answer)
- **C.** Complex addressing modes
- **D.** A small number of general-purpose registers
- **E.** Only LOAD and STORE operations interact with memory (Your Answer)

**Correct**

**Q.34)** N-window register file can only hold N procedure activations.

- **A.** True
- **B.** False (Your Answer)

**Correct**

**Q.35)** For which I/O arrangement does operation depend on an acknowledgement signal passing from the CPU to tell the interrupting device to place a self-identifying vector on the bus?

- **A.** Each Device has Unique Interrupt Input
- **B.** Software poll
- **C.** Daisy chain (Your Answer)
- **D.** Bus arbitration

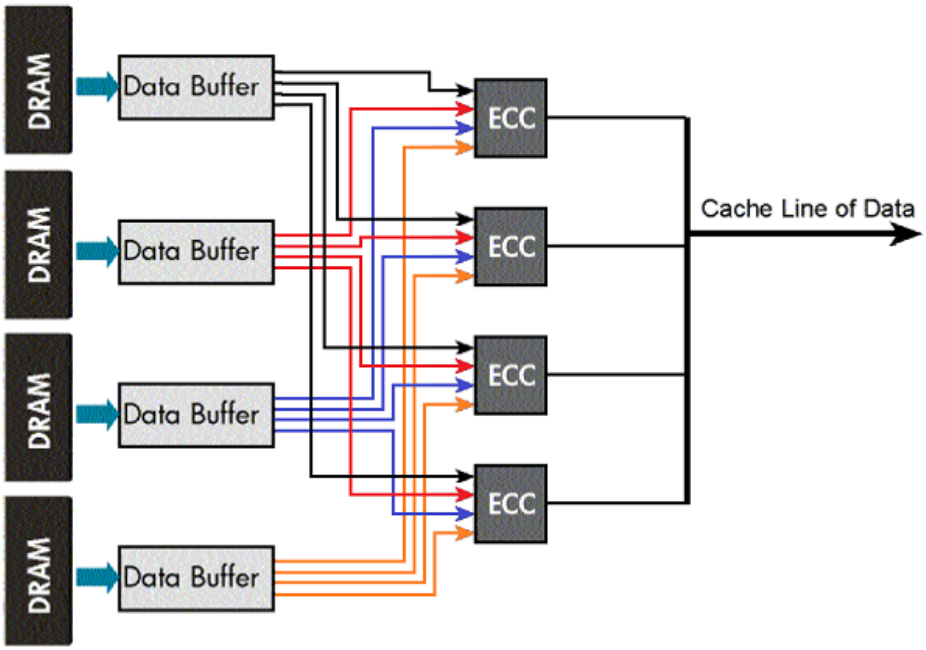
**Correct**

**Q.36)** What are the basic methods for improving register use? Select all that apply.

- **A.** Interrupts - uses a replacement algorithm to utilize full register access
- **B.** Hardware - creates more registers (Your Answer)
- **C.** Software - relies on compiler to maximize usage (Your Answer)

**Correct**

**Q.37)**




The figure above shows an error correction scheme that distributes the bits to be checked from a single DRAM across multiple error correcting circuits (ECCs) where it is checked against bits from other DRAMs.

- **A.** the error correction will be faster
- **B.** multiple error conditions usually occur in a single DRAM and distributing allows them to be corrected as single bit errors in multiple ECCs (Your Answer)
- **C.** it is necessary to use multiple ECCs to provide error correction across more than 8 bits

**D.** multiple ECCs can be implemented cheaper than a single ECC with a wider data bus

**Correct**

**Q.38)** In a single error correction system, if the stored data and parity bits had no errors, the binary representation of the syndrome word would be made from _____.

**A.** all ones

**B.** all zeros (Your Answer)
**C.** exactly one one and the rest zeros
**D.** two or more ones with the possibility of all ones
**E.** cannot be determined

**Correct**

**Q.39)** Which of the following I/O methods requires the CPU to act as a bridge for moving data between the I/O device and main memory? Select all that apply.

**A.** programmed I/O (Your Answer)
**B.** interrupt driven I/O (Your Answer)
**C.** direct memory access

**Correct**

**Q.40)** Where would you insert the NOOP in this code? (from Tarnoff's slide) _____ Address

| Instruction | | | |
|---|---|---|---|
| LOAD X,A | 100 | ADD 1,A | 101 |
| JUMP 105 | 102 | ADD A,B | 103 |
| SUB C,B | 104 | STORE A,Z | 105 |
| | | | 106 |

**A.** between 101 and 102
**B.** between 102 and 103 (Your Answer)
**C.** between 103 and 104
**D.** between 104 and 105

**Correct**

**Q.41)** True/False: The number of bits allocated for the offset can be used to calculate the page size.

**A.** True (Your Answer)
**B.** False

**Correct**

**Q.42)** A page fault occurs when _____.

**A.** an error occurs while loading a page from the hard drive into a frame in physical memory
**B.** an application tries to access a page that belongs to a different process
**C.** an application tries to access a page that belongs to the kernel
**D.** an application tries to access an undefined page, i.e., a page that doesn't contain any data or code
**E.** an application tries to access a page that is not loaded into a frame in physical memory (Your Answer)

**Incorrect**

**Q.43)** For which I/O arrangement is the interrupt priority defined by the single ISR that is called by all interrupts?

**A.** Each Device has Unique Interrupt Input
**B.** Software poll (Correct Answer)

**C.** Daisy chain
**D.** Bus arbitration (Your Answer)

**Correct**

**Q.44)** The _____ operates similar to a RAM cache.

**A.** inverted page table
**B.** translation lookaside buffer (Your Answer)

**Correct**

**Q.45)** RISC machines are highly dependent upon register operations.

- **A.** True (Your Answer)
- **B.** False

**Correct**

**Q.46)**

| Bit ID | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| ID in binary | 1111 | 1110 | 1101 | 1100 | 1011 | 1010 | 1001 | 1000 | 0111 | 0110 | 0101 | 0100 | 0011 | 0010 | 0001 |
| Data bit | Not used | Not used | Not used | $D_7$ | $D_6$ | $D_5$ | $D_4$ | | $D_3$ | $D_2$ | $D_1$ | | $D_0$ | | |
| Check code bit | | | | | | | | $P_3$ | | | | $P_2$ | | $P_1$ | $P_0$ |

***For the next four questions, use the diagram shown above that describes the assigned syndrome values corresponding to eight data bits ($D_0$ through $D_7$) and four parity bits ($P_0$ through $P_3$).***

Repeat the previous question for the parity bit $P_0$.

- **A.** D0 (Your Answer)
- **B.** D1 (Your Answer)
- **C.** D2
- **D.** D3 (Your Answer)
- **E.** D4 (Your Answer)
- **F.** D5
- **G.** D6 (Your Answer)
- **H.** D7

**Correct**

**Q.47)** True/False: Page tables themselves can potentially span multiple pages.

- **A.** True (Your Answer)
- **B.** False

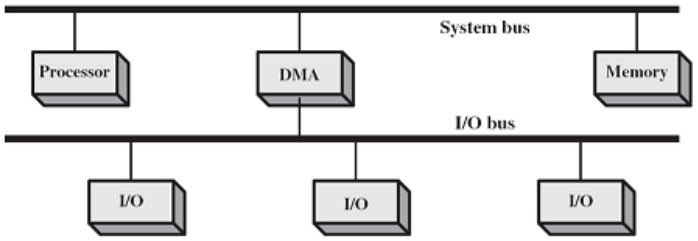
**Incorrect**

**Q.48)** Which type(s) of interrupt configurations depend on the physical (hardware) connections between the device and the CPU to determine the interrupt priority? Select all that apply.

- **A.** Separate interrupt pins for each device
- **B.** Daisy chain/hardware poll (Correct Answer)(Your Answer)
- **C.** Software poll (Your Answer)
- **D.** Bus arbitration (Your Answer)

**Correct**

**Q.49)**




I/O bus

In a configuration like the one shown above where the DMA controller acts as an interface between its I/O device(s) and the system bus, the DMA requires _____ access(es) to the bus to transfer a single word from the I/O device to memory.

**A.** 1 (Your Answer)
**B.** 2
**C.** 3
**D.** Cannot be predicted

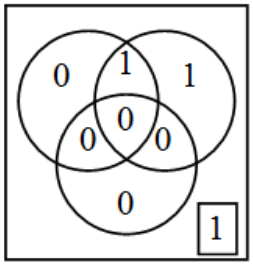
**Correct**

**Q.50)** Which of the following I/O methods places the least amount of burden on the processor? Select only one.

**A.** programmed I/O
**B.** interrupt-driven I/O
**C.** direct memory access (Your Answer)

**Correct**

**Q.51)**




Which of the following conditions does the above graphic of a 4-bit Hamming code depict?

**A.** No error
**B.** Single bit error (Your Answer)
**C.** Multiple bit errors

**Correct**

**Q.52)** The _____ requires a hash table to associate a physical frame with the page stored in it.

**A.** inverted page table (Your Answer)
**B.** translation lookaside buffer

**Correct**

**Q.53)** From the following list, identify all of the statements that are true regarding a system that uses paged virtual memory. Select all that apply.

**A.** Just like caches, virtual memory requires a replacement algorithm like LRU, LFU, FIFO, or random. (Your Answer)
**B.** With the possible exception of the last page, all pages of a process are of equal size. (Your Answer)
**C.** The process' logical page size is equal to the frame size of physical memory. (Your Answer)
**D.** All of the pages of a process must be loaded into memory.
**E.** When loaded into memory, the pages of a process must be in contiguous (adjacent or unbroken) frames in memory.
**F.** The offset bits (lower order bits) of a virtual/logical address are identical to the offset bits of the physical address. (Your Answer)