Plan Ahead
Today will cover cache coherence and sample questions on the test
11.29.12 - Test 3
12.4.12 - lecture on clusters
12.6.12 - cluster exercise in class
Final Exam is optional - Tuesday, December 11 - 1 pm to 3 pm

SMP
Symmetric Multi-Processor
Same speeds, same access to memory

MIMD
Tightly coupled - shared memory, high degree of interaction
Loosely coupled - clusters

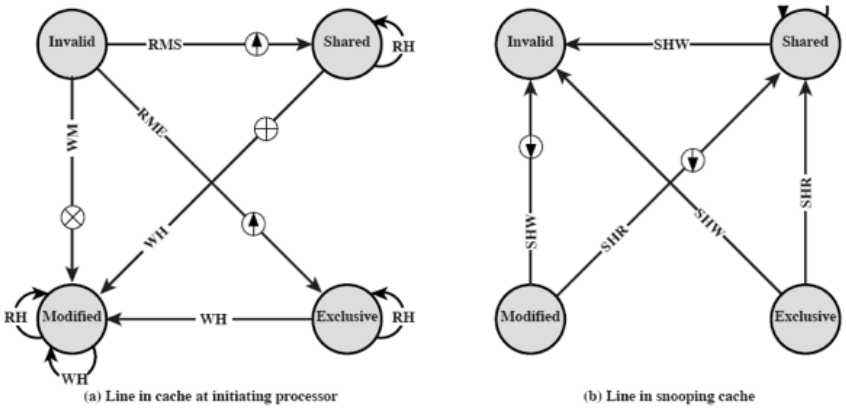
Cache Coherence
Can be solved with software or hardware
Hardware: central control & distributed control
Central control - directory protocol
Distributed control - snoopy protocol

Directory protocol: controller watches address lines and keep a table of who has which blocks and what the state of the data, when something is written, tell the others to invalidate those lines of cache. As long as you're reading write-through…
Problems - creates a central bottleneck and there is communication overhead
Most effective in large scale systems with complex interconnection schemes

Snoopy protocol:

Write Invalidate - MESI - a state is associated with every line
***M**odified*
***E**xclusive*
***S**hared*
***I**nvalid*

	M **Modified**	**E** **Exclusive**	**S** **Shared**	**I** **Invalid**
This cache line valid?	Yes	Yes	Yes	No
The memory copy is…	out of date	valid	valid	—
Copies exist in other caches?	No	No	Maybe	Maybe
A write to this line…	does not go to bus	does not go to bus	goes to bus and updates cache	goes directly to bus



(a) Line in cache at initiating processor

(b) Line in snooping cache

Write Update -